7 Sep 04

Amendments to the Specification:

Please insert the following paragraph after the paragraph beginning at page 6, line 16.

Figure 8 is a block diagram of a memory device that may be used in the computer system of Figure 7.

Please insert the following paragraphs after the paragraph beginning at page 16, line 20.

A memory device 430 are shown in block diagram form in Figure 8 can be substituted for the memory devices 401 of Figure 7. The memory device 430 includes a clock divider and delay circuit 440 that receives a master clock signal 442 and generates a large number of other clock and timing signals to control the timing of various operations in the memory device 430. The memory device 430 also includes a command buffer 446 and an address capture circuit 448 which receive an internal clock CLK signal, a command packet CA0-CA9 on a command bus 450, and a FLAG signal on line 452. The command packet contains control and address information for each memory transfer, and the FLAG signal identifies the start of a command packet. The command buffer 446 receives the command packet from the bus 450, and then provides the command to a command decoder and sequencer 460. The command decoder and sequencer 460 generates a large number of internal control signals to control the operation of the memory device 430 during a memory transfer corresponding to the command. The address capture circuit 448 also receives the command packet from the command bus 450 and outputs a 20-bit address corresponding to the address information in the command. The address is provided to an address sequencer 464 which generates a corresponding 3-bit bank address on bus 466, an 11-bit row address on bus 468, and a 6-bit column address on bus 470.

The memory device 430 shown in Figure 8 includes a plurality of memory banks 480, in this case eight memory banks 480a-h. After a memory read from one bank 480a, the bank 480a can be precharged while the remaining banks 480b-h are being accessed. Each of the memory banks 480a-h receives a row address from a respective row latch/decoder/driver 482a-h. All of the row latch/decoder/drivers 482a-h receive the same row address from a predecoder 484 which, in turn, receives a row address from either a row address register 486 or a refresh counter

The command buffer 446 includes a clock generator circuit 447 according to an embodiment of present invention to generate the clock signal for synchronizing receipt of the command packets from the command bus 4

488 as determined by a multiplexer 490. However, only one of the row latch/decoder/drivers 482a-h is active at any one time as determined by bank control logic 494 as a function of bank data from a bank address register 496.

The column address on bus 470 is applied to a column latch/decoder 500 which, in turn, supplies I/O gating signals to an I/O gating circuit 502. The I/O gating circuit 502 interfaces with columns of the memory banks 480a-h through sense amplifiers 504. Data is coupled to or from the memory banks 480a-h through the sense amps 504 and I/O gating circuit 502 to a data path subsystem 508 which includes a read data path 510 and a write data path 512. The read data path 510 includes a read latch 520 receiving and storing data from the I/O gating circuit 502. In the memory device 430 shown in Figure 8, 64 bits of data are applied to and stored in the read latch 520. The read latch then provides four 16-bit data words to a multiplexer 522. The multiplexer 522 sequentially applies each of the 16-bit data words to a read FIFO buffer 524. Successive 16-bit data words are clocked through the FIFO buffer 524 by a clock signal generated from an internal clock by a programmable delay circuit 526. The FIFO buffer 524 sequentially applies the 16-bit words and two clock signals (a clock signal and a quadrature clock signal) to a driver circuit 528 which, in turn, applies the 16-bit data words to a data bus 530 forming part of the processor bus 414. The driver circuit 528 also applies the clock signals to a clock bus 532 so that a device such as the processor 402 (Figure 7) reading the data on the data bus 530 can be synchronized with the data.

The write data path 512 includes a receiver buffer 540 coupled to the data bus 530. The receiver buffer 540 sequentially applies 16-bit words from the data bus 530 to four input registers 542, each of which is selectively enabled by a signal from a clock generator circuit 544. Thus, the input registers 542 sequentially store four 16-bit data words and combine them into one 64-bit data word applied to a write FIFO buffer 548. The write FIFO buffer 548 is clocked by a signal from the clock generator 544 and an internal write clock WCLK to sequentially apply 64-bit write data to a write latch and driver 550. The write latch and driver 550 applies the 64-bit write data to one of the memory banks 480a-h through the I/O gating circuit 502 and the sense amplifier 504.